

AMENDMENT TO THE CLAIMS

Claim 1-20 Canceled

21. (currently amended) An electrically programmable memory element, comprising:

a substrate;

a first dielectric layer formed over said substrate;

a first conductive layer formed over said first dielectric layer and in electrical communication with said substrate;

a second dielectric layer formed over said first conductive layer, said second dielectric layer having an opening therethrough to said first conductive layer;

a spacer disposed about a peripheral portion of said opening to form a pore, said pore overlying said first dielectric layer;

a programmable resistance material disposed within said pore and in electrical communication with said first conductive layer; and

a second conductive layer formed over in electrical communication with said programmable resistance material.

22. (currently amended) The memory element of claim 21, wherein said spacer is formed by the method comprising the steps of:

forming a third dielectric layer over a peripheral portion of ~~ef~~ said opening; and

removing a portion of said third dielectric layer.

23. (currently amended) The memory element of claim 21, further comprising:

a third conductive layer electrically coupled between said first conductive layer and a said substrate, wherein substantially all electrical communication between said ~~second conductive layer~~ substrate and said first conductive layer is through an edge portion of said third conductive layer.

24. (original) The memory element of claim 23, wherein said third conductive layer comprises a sidewall layer.

25. (original) The memory element of claim 23, wherein said third conductive layer is a conductive sidewall spacer or a conductive sidewall liner.

26. (original) The memory element of claim 21, wherein said programmable resistance material comprises a phase change material.

27. (original) The memory element of claim 21, wherein said programmable resistance material comprises a chalcogen element.

Claim 28-60 Canceled

61. (new) An electrically operated memory element comprising:

a substrate;

a first dielectric layer formed over said substrate, said first dielectric layer having an opening therethrough;

a first conductive layer lining the sidewall surface of the opening of said first dielectric layer, said first

conductive layer in electrical communication with said substrate;

a second dielectric layer formed over said first conductive layer within said opening;

a second conductive layer formed over a top surface of said first conductive layer and a top surface of said second dielectric layer;

a third dielectric layer formed over said second conductive layer, said third dielectric layer having a pore therethrough, said pore overlying said second dielectric layer; and

a programmable resistance material disposed in said pore and in electrical communication with said second conductive layer.

62. (new) The memory element of claim 61, wherein the resistivity of said second conductive layer is greater than the resistivity of said first conductive layer.

63. (new) The memory element of claim 61, wherein said first conductive layer is formed over a portion of the bottom surface of said opening in said first dielectric layer, said portion being less than the entire bottom surface of said opening.

64. (new) The memory element of claim 61, wherein said first conductive layer is cup-shaped.

65. (new) The memory element of claim 61, wherein said programmable resistance material is a phase-change material.